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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,048	06/24/2003	Jason J. Payne	1826-US	1882

7590 11/18/2005

Teradyne, Inc.
Legal Department
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,048	PAYNE ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-19* is/are allowed.

6)☒ Claim(s) *1-4 and 6-8* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 17 October 2005 has been entered. Applicants have amended the specification, drawings, and claims 9-12, 14, and 16.

Drawings

2. The drawing was received on 17 October 2005. The drawing is approved.

Specification

3. The specification, page 2, was also received. Applicants' arguments have been fully considered and are persuasive. The specification is approved.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda (U.S. Patent 5,331,514).

Regarding claim 1, Kuroda, as can be seen in figures 1, 2, and 5, discloses a PCB having a surface providing a mating interface to which is electrically connected an electrical component having signal conductors 3S(3) and ground conductors 3G(3), see column 2, lines 28-32 and lines 44-49. The PCB comprising:

(a) A plurality of stacked dielectric layers 2 with a conductor 3S(3) and 3G(3) exposed on at least one of the plurality of the layers, see column 1, lines 41-43, and column 2, lines 44-49,

(b) a mating interface including:

(c) a plurality of conductive vias 3 aligned in a repeating pattern of a square so forming a plurality of rows of squares, see figure 5 and column 1, lines 49-52,

(d) the plurality of conductive vias 3 extending through at least a portion of the plurality of the layers 2, at least one of the plurality of conductive vias 3 intersecting the conductor, see column 2, line 68-continuing column 3, lines 1-8,

(e) the plurality of conductive vias 3 including signal conductor connecting conductive vias 3S and ground conductor connecting conductive vias 3G, see column 2, lines 44-49, and

(f) for each of plurality of rows of the conductive vias 3, there are at least twice as many ground conductor connecting conductive vias 3G as signal conductor connecting conductive vias 3S and the conductive vias 3 are positioned relative to one another so that for each signal conductor connecting conductive via 3S, there are ground conductor connecting conductive vias 3G adjacent either side of the signal conductor connecting conductive via 3S, see column 1, lines 50-53.

Regarding claim 2, Kuroda discloses the vias that can be arranged in a rectangular pattern instead of a square pattern so forming rows of vias along the width sides of the rectangular, see column 4, lines 9-17. Since the width of a rectangular is shorter than the length, therefore the distance between the signal conductor connecting conductive via 3S and the adjacent ground conductor connecting conductive via 3G of a row is always less than the distance between adjacent rows of the conductive vias 3.

Regarding claim 3, Kuroda discloses the vias that can be arranged in a square or a rectangular pattern, as explained in claims 1 and 2 above. In a square pattern, the distance between a signal conductor connecting conductive via 3S and an adjacent ground conductor connecting conductive via 3G on one side is similar to a distance between the signal conductor connecting conductive via 3S and an adjacent ground conductor connecting conductive via 3G on the other side.

Regarding claim 4, as can be seen in figure 2, Kuroda discloses a surface mounting pad (no number) disposed on each of the plurality of conductive vias 3, the signal conductor 3S(3) and ground conductor 3G(3) of the electrical component being electrically connected to the surface mounting pads. The surface mounting pads are the top conductive surface of the vias that the component is attached to.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Uematsu et al. (U.S. Patent 6,787,710 B2).

Regarding claim 6, Kuroda discloses every limitation as shown in claim 1 above including a ground plane layer (no number) and a power plane layer, see column 1, lines 39-43, but failed to disclose that each signal conductor connecting conductive via

of the ground plane layer, there is provided an area surrounding the signal conductor connecting conductive via that is free of the ground plane layer.

Uematsu et al. disclose a PCB having conductive vias 10 and 11 extending through a multilayer substrate, which includes a ground plane layer 2 and an area 14 (insulating portions) surrounding the vias that is free of the layers, see figure 1 and column 3, lines 19-20.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the insulating portion as taught by Uematsu et al. in the PCB of Kuroda for preventing short circuit between the signal conductor connecting conductive via and the ground layer.

Regarding claim 7, as can be seen in Kuroda's figure 1 and further in view of Uematsu et al., and as explained in claim 6 above, each ground conductor connecting conductive via of the ground plane layer, there is provided at least one discrete area adjacent the ground conductor connecting conductive via that is free of the ground plane layer, which is the insulating portion provided by signal conductor connecting conductive via.

Regarding claim 8, Kuroda in view of Uematsu et al., discloses every limitation as shown in claims 1, 6, and 7 above, in the same manner as described in claims 6 and 7 where the power plane layer is in place of ground plane layer.

Response to arguments

8. Applicants' arguments filed on 17 October 2005 related to claims 9-19 have been fully considered and are persuasive. The rejection of claims 9-19 has been withdrawn.

The arguments related to claims 1-4, 6-8 have been also fully considered and are not persuasive.

(a) Regarding the "Kuroda describes an integrated circuit package. It does not describe a printed circuit board having a plurality of stacked dielectric layers as recited in claim 1",

Kuroda discloses an integrated circuit package, which is inherently a printed circuit board. Furthermore, there is no different between an integrated circuit package and a printed circuit board, and Kuroda also discloses a stacked of dielectric layers, see column 1, lines 41-43.

(b) Regarding the ".... a plurality of rows of conductive vias..... there are at least twice as many ground conductor connecting conductive vias as signal conductor connecting conductive vias for each of the plurality of rows of the conductive vias.....",

Kuroda discloses rows of square pattern. In each square, there are at least twice as many ground conductor conductive vias as signal conductor connecting conductive vias for each of the plurality of rows of the conductive vias.

(c) Regarding "the conductive vias are positioned relative to one another so that for each signal conductor connecting conductive via, there are ground conductor connecting conductive vias adjacent either side of the signal conductor connecting conductive via.",

As shown in figure 5, every signal conductor connecting conductive via has ground conductor connecting conductive vias adjacent either side of the signal conductor connecting conductive via.

(d) Regarding "a plurality of conductive vias aligned in a plurality of rows. Rows of squares do not meet the claim limitation".

The claim itself does not limit a row as a single line of vias or pads; therefor a row can be broadly interpreted as a group of squares arranged in a row wherein a row is not necessary a single line but a multiple of lines.

(e) Regarding the " ..... unreasonable interpretation of the term vias",

Kuroda clearly disclose the vias (holes), and bumps (conductors) electrically coupled to the ends of each holes, see column 2 line 68 continuing to column 3, line 9 and column 2, lines 54-62.

Allowable Subject Matter

9. Claim 5 is objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all the limitations of the base claims and any intervening claims.

10. Claims 9-19 are allowed.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
1 November 2005

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